REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-10 and 12-18 are in this application. Claims 1 and 12 have been amended. Claim 11 has been cancelled. Claims 15-18 have been added to alternately and additionally claim the present invention.

The Examiner rejected claims 1-3, 5, 8, 10 and 12-13 under 35 U.S.C. §102(b) as being anticipated by Brown (U.S. Patent No. 5,939,767). The Examiner also rejected claims 4, 6, 7, 9, and 11 under 35 U.S.C. §103(a) as being unpatentable over Brown. For the reasons set forth below, applicant respectfully these rejections as applied to amended claim 1.

Claim 1 recites, in part,

> "a well region of a second conductivity type disposed in the semiconductor substrate, the well region having a floating potential."

Claim 12 recites similar limitations.

Support for the addition of the phrase "the well region having a floating potential" is provided in applicant's FIG. 8A which shows ESD protection structure 100 having only an anode and a cathode. Since no other connection to structure 100 is shown, the well must have a floating potential.

In rejecting the claims, the Examiner pointed to the n-well shown in FIG. 27 of Brown as constituting the well region of claim 1. FIG. 27 of the Brown reference, however, does not teach or suggest that the n-well in FIG. 27 has a floating potential.

As shown in FIG. 27, Brown teaches that the potential on the n-well is set by the voltage on the input pad via the n+ contact region. As a result, it is not possible for the n-well in FIG. 27 of Brown to have a floating potential. Thus, claims 1-3, 5, 8, 10 and 12-13 are not anticipated by Brown. Similarly, claims 4, 6, 7, and 9, which directly or indirectly depend from claim 1, are patentable over Brown for the same reasons.

New claim 15 recites, in part,

> "a well region of the second conductivity type formed in the semiconductor material, the well region contacting the isolation region, being spaced apart from the

first region, having a dopant concentration that is less than the dopant concentration of the first region, and not contacting a region of the second conductivity type that has a dopant concentration that is greater than the dopant concentration of the well region."

FIG. 27 of Brown, however, does not teach a well region that has a dopant concentration that is less than the dopant concentration of the first region, and does not contact a region of the second conductivity type that has a dopant concentration that is greater than the dopant concentration of the well region.

As shown in FIG. 27 of Brown, if the n+ region connected to INPUT or the n+ region that lies under the STI region is read to be a part of the n-well, then the n-well fails to satisfy the requirement that the dopant concentration of the well be less than the dopant concentration of the first region. On the other hand, if the n+ regions are not read to be part of the n-well, then the n-well fails to satisfy the requirement that the n-well not contact a region of the second conductivity type that has a dopant concentration that is greater than the dopant concentration of the well region.

As a result, new claim 15 is patentable over Brown. In addition, since claims 16-18 depend either directly or indirectly from claim 15, claims 16-18 are patentable over Brown for the same reasons as claim 15.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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APPENDIX

In the Claims

Please cancel claim 11.

Please amend the claims as follows:

1. (Twice Amended) An ESD protection structure for an integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a well region of a second conductivity type disposed in the semiconductor substrate, the well region having a floating potential;

a first region of the first conductivity type disposed in the well region on the semiconductor substrate;

a second region of the second conductivity type disposed in and on the semiconductor substrate and spaced apart from the first region and the well; and

an electrical isolation region disposed in the semiconductor substrate between the first region and the second region.

12. (Amended) An ESD protection structure formed in a semiconductor material of a first conductivity type, the structure comprising:

a well region of a second conductivity type formed in the semiconductor material, the well region having a floating potential;

a first region of the first conductivity type formed in the well region;

a second region of the second conductivity type formed in the semiconductor material and spaced apart from the first region and the well; and

an electrical isolation region formed in the semiconductor [substrate] material between the first region and the second region.

Claims 15-18 have been added.